

MIL-STD-1553 / 1760 3.3V Dual Transceiver with Integrated IP Security Module

April 2022

DESCRIPTION

The HI-1587 is an ultra-low power MIL-STD-1553 dual transceiver designed to meet all requirements of the MIL-STD-1553 and MIL-STD-1760 specifications. The device is designed to provide the transceiver interface between the bus isolation transformers and an FPGA with instantiated Holt IP and features an integrated IP security module necessary to enable the IP. This eliminates the need for a traditional external IP dongle chip, commonly used with other IP solutions.

The HI-1587 is also the first MIL-STD-1553 transceiver to feature 1.8V, 2.5V and 3.3V compatible digital I/O, making it easier to interface with a broad range of FPGAs.

The transmitter takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each bus. The receiver section of the each bus converts the 1553 bus bi-phase analog signals to complementary CMOS / TTL data suitable for input to the IP Core Manchester decoder.

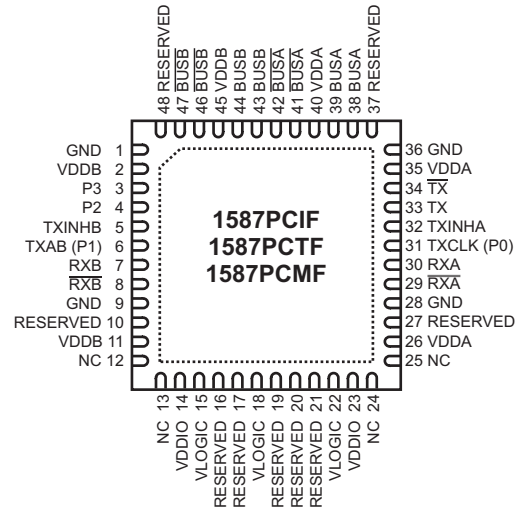
FEATURES

- Compliant to MIL-STD-1553A and B, MIL-STD-1760
- 3.3V single supply operation for 3.3V systems
- 1.8V, 2.5V and 3.3V compatible digital I/O
- Smallest transceiver footprint available in 6mm x 6mm 48-pin plastic chip-scale package (QFN)
- Includes integrated MIL-STD-1553 IP security module

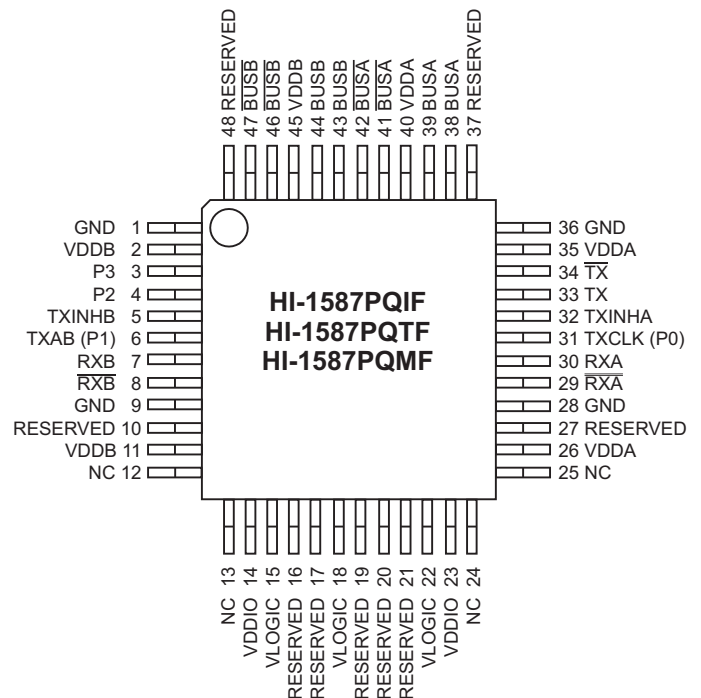
APPLICATIONS

- MIL-STD-1553 Terminals
- Flight Control and Monitoring
- Radar Systems
- ECCM Interfaces
- Stores Management
- Test Equipment
- Sensor Interfaces
- Instrumentation

PIN CONFIGURATION



**48 Pin Plastic 6mm x 6mm
Chip-Scale Package (QFN)**



44 - Pin Plastic Quad Flat Pack (PQFP)

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	GND	power supply	Ground
2	VDDDB	power supply	+3.3 volt power for transceiver B
3	P3	digital input	Connect to IP output P3 on FPGA. Internal pull-down resistor
4	P2	digital output	Connect to IP input P2 on FPGA.
5	TXINHB	digital input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled. Internal pull-down resistor
6	TXAB (P1)	digital input	Transmit select (BUSA or BUSB). Connect to IP output P1 on FPGA. TXAB = 0 selects BUSA. TXAB = 1 selects BUSB. Internal pull-down resistor
7	RXB	digital output	Receiver B output, non-inverted
8	$\overline{\text{RXB}}$	digital output	Receiver B output, inverted
9	GND	power supply	Ground
10	RESERVED	-	MUST be open-circuit. DO NOT connect.
11	VDDDB	power supply	+3.3 volt power for transceiver B
12	NC	-	Not Connected
13	NC	-	Not Connected
14	VDDIO	power supply	Power for digital I/O. Supports 1.8V, 2.5V or 3.3V.
15	VLOGIC	power supply	+3.3 volt power for digital logic
16	RESERVED	-	MUST be open-circuit. DO NOT connect.
17	RESERVED	-	MUST be open-circuit. DO NOT connect.
18	VLOGIC	power supply	+3.3 volt power for digital logic
19	RESERVED	-	MUST be open-circuit. DO NOT connect.
20	RESERVED	-	MUST be open-circuit. DO NOT connect.
21	RESERVED	-	MUST be open-circuit. DO NOT connect.
22	VLOGIC	power supply	+3.3 volt power for digital logic
23	VDDIO	power supply	Power for digital I/O. Supports 1.8V, 2.5V or 3.3V.
24	NC	-	Not Connected
25	NC	-	Not Connected
26	VDDA	power supply	+3.3 volt power for transceiver A
27	RESERVED	-	MUST be open-circuit. DO NOT connect.
28	GND	power supply	Ground
29	$\overline{\text{RXA}}$	digital output	Receiver A output, inverted
30	RXA	digital output	Receiver A output, non-inverted
31	TXCLK (P0)	digital input	Transmit clock. Connect to IP output P0 on FPGA. Internal pull-down resistor
32	TXINHHA	digital input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled. Internal pull-down resistor
33	TX	digital input	Transmitter digital data input, non-inverted. Internal pull-down resistor
34	$\overline{\text{TX}}$	digital input	Transmitter digital data input, inverted. Internal pull-down resistor
35	VDDA	power supply	+3.3 volt power for transceiver A
36	GND	power supply	Ground
37	RESERVED	-	MUST be open-circuit. DO NOT connect.
38	BUSA	analog output	MIL-STD-1553 bus driver A, positive signal
39	BUSA	analog output	MIL-STD-1553 bus driver A, positive signal
40	VDDA	power supply	+3.3 volt power for transceiver A
41	$\overline{\text{BUSA}}$	analog output	MIL-STD-1553 bus driver A, negative signal
42	$\overline{\text{BUSA}}$	analog output	MIL-STD-1553 bus driver A, negative signal
43	BUSB	analog output	MIL-STD-1553 bus driver B, positive signal
44	BUSB	analog output	MIL-STD-1553 bus driver B, positive signal
45	VDDDB	power supply	+3.3 volt power for transceiver B
46	$\overline{\text{BUSB}}$	analog output	MIL-STD-1553 bus driver B, negative signal
47	$\overline{\text{BUSB}}$	analog output	MIL-STD-1553 bus driver B, negative signal
48	RESERVED	-	MUST be open-circuit. DO NOT connect.

Table 1. Pin Descriptions

BLOCK DIAGRAM

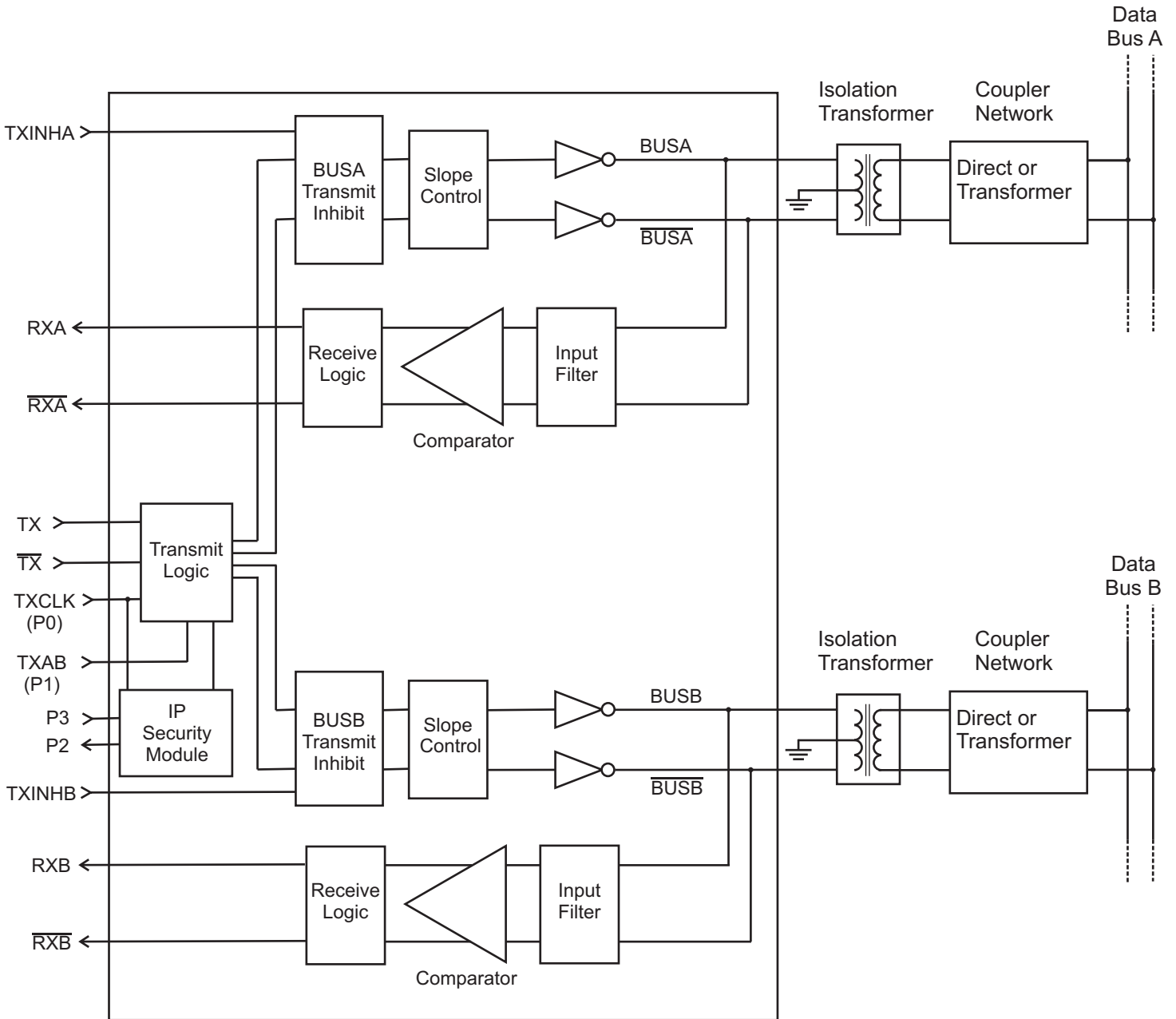


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION

The HI-1587 dual MIL-STD-1553 bus transceiver contains a differential voltage source driver and a differential analog bus receiver for each bus. It is designed for applications using a MIL-STD-1553B communications bus. The device generates a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the HI-1587 transmitter is a pair of complementary CMOS inputs TX and $\overline{\text{TX}}$. The transmission bus (BUSA or BUSB) is selected by asserting the TXAB (P1) pin (TXAB = 0 for Bus A, TXAB = 1 for Bus B). The transmitter accepts Manchester II bi-phase data and converts it to differential analog voltages on BUSA and $\overline{\text{BUSA}}$, or BUSB and $\overline{\text{BUSB}}$. The transceiver outputs are either direct- or transformer-coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 Volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when TX and $\overline{\text{TX}}$ are both driven to the same logic state. A bus transmitter is also forced to the high impedance state when logic "1" is applied at the TXINHA (or TXINHB) transmit inhibit input, regardless of the TX and $\overline{\text{TX}}$ input condition.

RECEIVER

The receiver accepts bi-phase differential analog signals from the MIL-STD-1553 bus through the same direct- or transformer-coupled interface at the BUSA and $\overline{\text{BUSA}}$ (or BUSB and $\overline{\text{BUSB}}$) pins. The receiver differential input stage drives a filter and threshold comparator to produce CMOS data at the RXA and $\overline{\text{RXA}}$ (or RXB and $\overline{\text{RXB}}$) output pins.

MIL-STD-1553 BUS INTERFACE

A direct-coupled interface (see Figure 2) uses a 1:2.65 turns-ratio isolation transformer and two 55 ohm isolation resistors between the transformer and the bus. The primary center-tap of the isolation transformer must be connected to GND.

In a transformer-coupled interface (see Figure 2), the transceiver is connected to a 1:2.07 turns-ratio isolation transformer which is connected to the main bus using a 1:1.4 turns-ratio coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Z_0) between the coupling transformer and the bus.

Figure 3 and Figure 4 show test circuits for measuring electrical characteristics of both direct- and transformer-coupled interfaces respectively. (See electrical characteristics on the following pages).

IP Security Module

The HI-1587 features an integrated IP security module, eliminating the need for an external dongle chip commonly used by other IP solutions. The security module is necessary to enable Holt's proprietary MIL-STD-1553 protocol IP. A unique key is factory programmed for each transceiver. Upon reset, an instantiated FPGA IP will send a security handshake request to the transceiver, which must respond appropriately to enable the IP.

Power Supply Sequencing

The power supply sequencing of VDDA/VDDDB versus VDDIO should be controlled to prevent large currents during turn-on and turn-off. The recommended sequence is VDDA/VDDDB followed by VDDIO, always ensuring that VDDA/VDDDB is the most positive supply within 1ms.

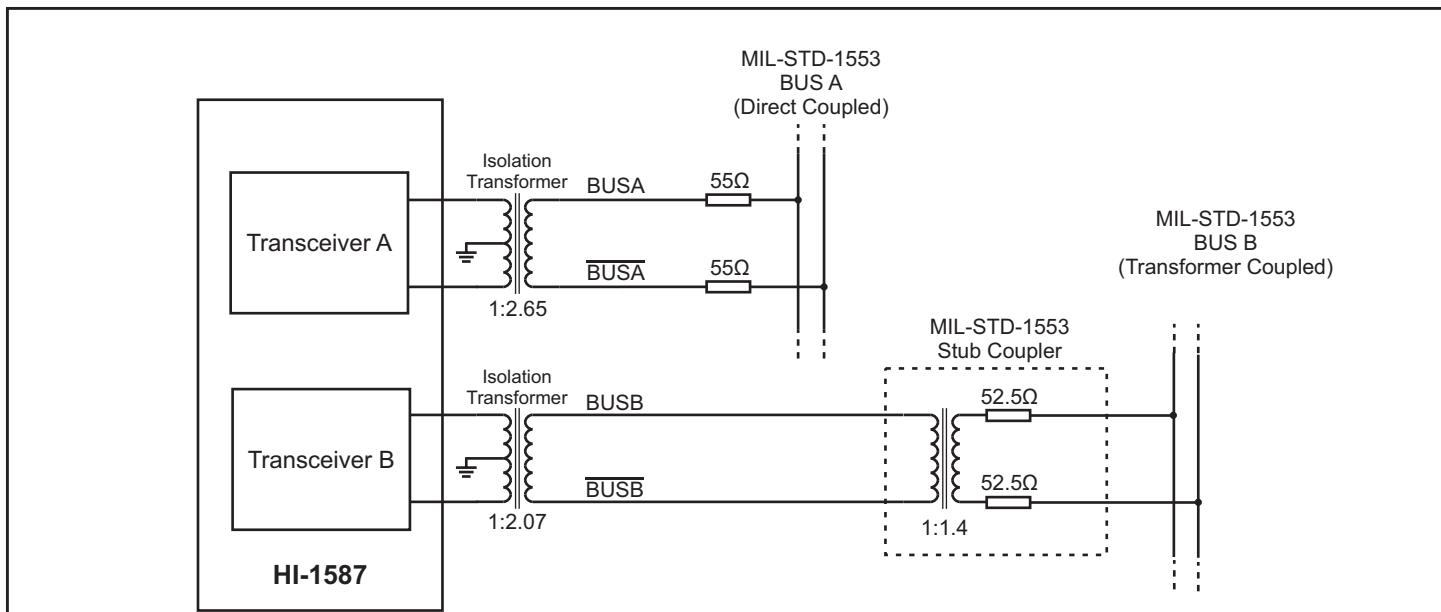
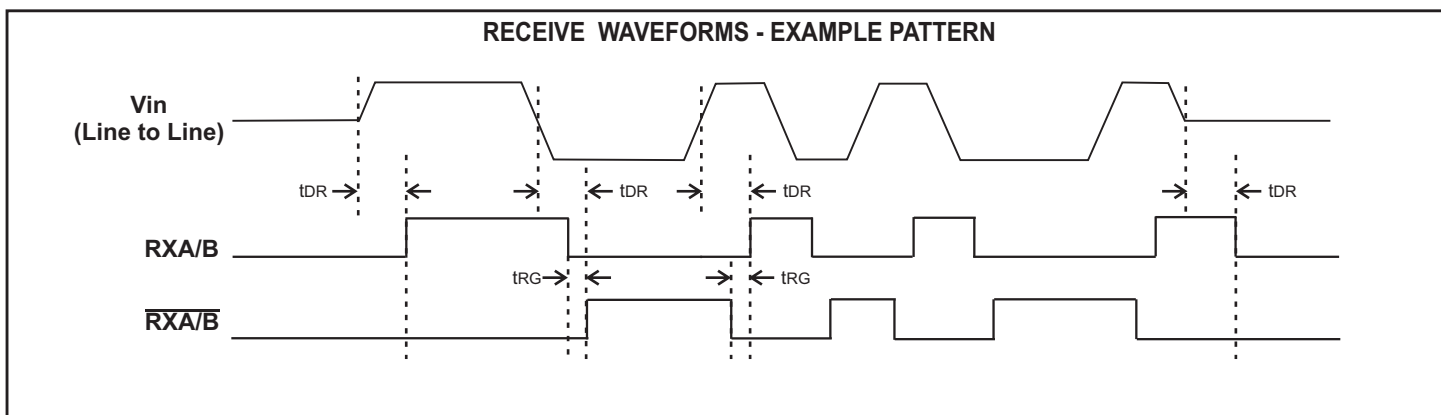
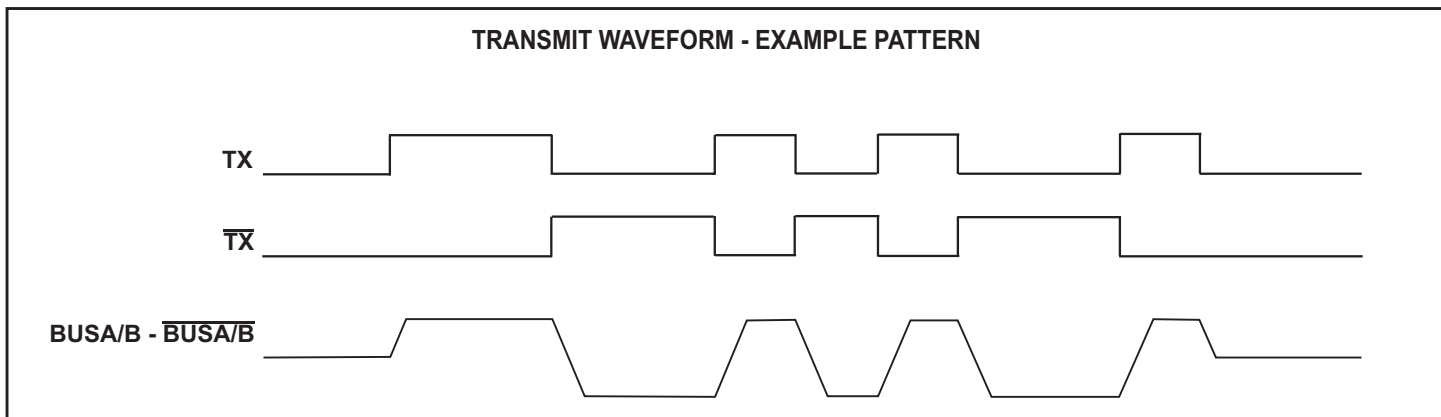


Figure 2. Bus Connection Example



ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +5 V
Logic input voltage range	-0.3 V dc to +3.6 V
Voltage at BUSA/B or $\overline{\text{BUSA/B}}$ pins	+/-7 V
VDDIO – VLOGIC	0.5V
Reflow Solder Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
VDD	3.3V... ±5%
VLOGIC	3.3V... ±10%
VDDIO ≤	VLOGIC
Temperature Range	
Industrial	-40°C to +85°C
Hi-Temp	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VDD = 3.14 V to 3.46V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Transceiver Supply Voltage	VDD		3.14	3.30	3.46	V
Total Supply Current	ICC1	Not Transmitting		25	30	mA
	ICC2	Transmit one bus @ 50% duty cycle, 78 Ω resistive load		300	330	mA
	ICC3	Transmit one bus @ 100% duty cycle, 78 Ω resistive load		620	670	mA
Power Dissipation	PD1	Not Transmitting		83	104	mW
	PD2	Transmit one bus @ 100% duty cycle, 78 Ω resistive load		830	970	mW
Logic Supply Voltage	VLOGIC		3.0	3.30	3.6	V
Logic Supply Current	ILOGIC				5.0	mA
Digital I/O Supply Voltage	VDDIO	1.8V Digital I/O	1.65	1.8	1.95	V
		2.5V Digital I/O	2.3	2.5	2.7	V
		3.3V Digital I/O	3.0	3.3	3.6	V
Digital I/O Supply Current	IVDDIO			15	mA	
Min. Input Voltage (High)	VIH	Digital inputs, VDDIO = VDD = 3.3V	70%			VDD
Max. Input Voltage (Low)	VIL	Digital inputs, VDDIO = VDD = 3.3V			30%	VDD
Min. Output Voltage (High)	VOH	Iout = -1.0mA, Digital outputs VDDIO = VDD = 3.3V	90%			VDD
Max. Output Voltage (Low)	VOL	Iout = 1.0mA, Digital outputs VDDIO = VDD = 3.3V			10%	VDD
Min. Input Voltage (High)	VIH	Digital inputs, VDDIO = 2.5V, VDD = 3.3V	1.7			V
Max. Input Voltage (Low)	VIL	Digital inputs, VDDIO = 2.5V, VDD = 3.3V			0.7	V
Min. Output Voltage (High)	VOH	Iout = -1.0mA, Digital outputs VDDIO = 2.5V, VDD = 3.3V	2.3			V
Max. Output Voltage (Low)	VOL	Iout = 1.0mA, Digital outputs VDDIO = 2.5V, VDD = 3.3V			0.2	V

DC ELECTRICAL CHARACTERISTICS (cont.)

V_{DD} = 3.14 V to 3.46V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Min. Input Voltage (High)	V _{IH}	Digital inputs, V _{DDIO} = 1.8V, V _{DD} = 3.3V	1.17			V
Max. Input Voltage (Low)	V _{IL}	Digital inputs, V _{DDIO} = 1.8V, V _{DD} = 3.3V			0.63	V
Min. Output Voltage (High)	V _{OH}	I _{OUT} = -1.0mA, Digital outputs V _{DDIO} = 1.8V, V _{DD} = 3.3V	1.35			V
Max. Output Voltage (Low)	V _{OL}	I _{OUT} = 1.0mA, Digital outputs V _{DDIO} = 1.8V, V _{DD} = 3.3V			0.45	V
Min. Input Current (High)	I _{IH}	All Digital inputs, Internal Pull-Downs	20	30	50	μA
Max. Input Current (Low)	I _{IL}	All Digital inputs	-20			μA
RECEIVER(Measured at Point "Ad" in Figure 3 unless otherwise specified)						
Input resistance	R _{IN}	Differential (at chip pins)	5			kOhm
Input capacitance	C _{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V _{ICM}		-10.0		10.0	V-pk
Threshold Voltage - Direct-coupled	Detect	V _{THD}	1.15			Vp-p
	No Detect	V _{THND}			0.28	Vp-p
Theshold Voltage - Transformer-coupled	Detect	V _{THD}	0.86			Vp-p
	No Detect	V _{THND}			0.20	Vp-p
TRANSMITTER(Measured at Point "Ad" in Figure 3 unless otherwise specified)						
Output Voltage	Direct coupled	V _{OUT}	6.0		9.0	Vp-p
	Transformer coupled	V _{OUT}	20.0		27.0	Vp-p
Output Noise		V _{ON}			10.0	mVp-p
Output Dynamic Offset Voltage	Direct coupled	V _{DYN}	-90		90	mV
	Transformer coupled	V _{DYN}	-250		250	mV
Output Capacitance		C _{OUT}			15	pF

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.14 V to 3.46 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "AT" in Figure 4 unless otherwise specified)						
Receiver Delay	t _{DR}	From input zero crossing to RXA/B or $\overline{\text{RXA/B}}$			450	ns
Receiver gap time	t _{RG}	Spacing between RXA/B and $\overline{\text{RXA/B}}$ pulses. 1 MHz sine wave applied at point "AT" Figure 4, amplitude range 0.86 V _{p-p} to 27.0V _{p-p}	90		365	ns
TRANSMITTER (Measured at Point "AT" in Figure 4)						
Driver Delay	t _{DT}	TX, $\overline{\text{TX}}$ to BUSA/B, $\overline{\text{BUSA/B}}$			160	ns
Rise time	t _r	70 ohm load	100	150	300	ns
Fall Time	t _f	70 ohm load	100	150	300	ns
Inhibit Delay	t _{DI-H}	Inhibited output			100	ns
	t _{DI-L}	Active output			150	ns
Tx/ $\overline{\text{Tx}}$ data set-up time to CLK rising edge	t _{Tx-S}	ENCLK pin enabled (high)	10			ns
Tx/ $\overline{\text{Tx}}$ data hold time after CLK rising edge	t _{Tx-H}	ENCLK pin enabled (high)	10			ns

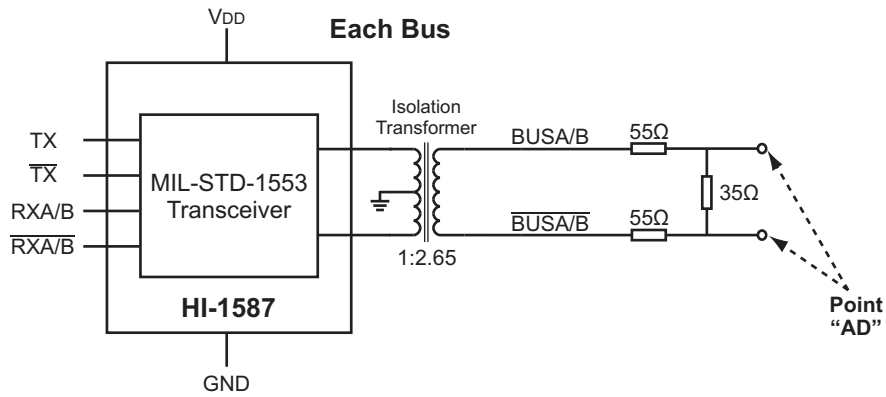


Figure 3. Direct Coupled Test Circuit

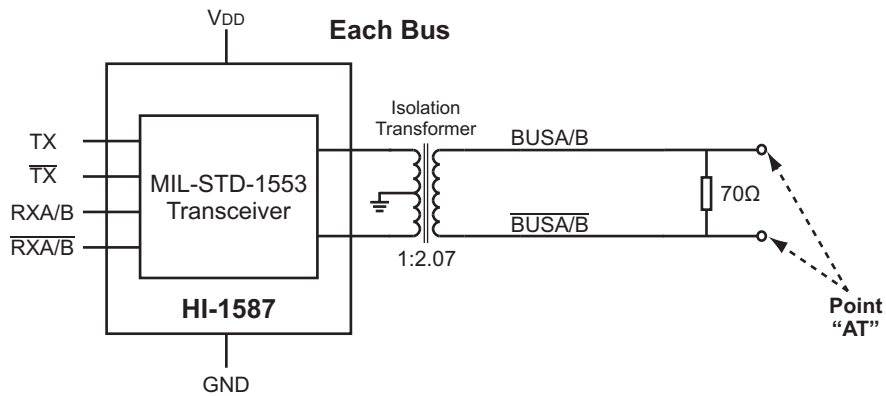


Figure 4. Transformer Coupled Test Circuit

HEAT SINK

The HI-1587PCI/T/M uses a plastic chip-scale package (QFN). These packages include a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board ground plane or left floating.

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

ORDERING INFORMATION

HI - 1587 PC x F - xxx X

PART #	DEVICE FUNCTIONALITY
B	Pairs with HI-6300-xxxB – (Holt RT/MT IP Core)
C	Pairs with HI-6300-xxxC – (Holt BC/RT IP Core)
D	Pairs with HI-6300-xxxD – (Holt BC/RT/MT IP Core)
F	Pairs with HI-6300-xxxF – (Holt DO-254 DAL A Compliant RT/MT IP Core)
G	Pairs with HI-6300-xxxG – (Holt DO-254 DAL A Compliant BC/RT IP Core)
H	Pairs with HI-6300-xxxH – (Holt DO-254 DAL A Compliant BC/RT/MT IP Core)

CUSTOMER ID
Unique 3-digit customer project code, e.g. 001, 002, 003, etc.

PART #	LEAD FINISH
F	NiPdAu (Pb-free RoHS compliant)

PART #	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART #	PACKAGE DESCRIPTION
PC	48 PIN PLASTIC CHIP-SCALE PACKAGE QFN (48PCS6)

ORDERING INFORMATION

HI - 1587 PQ x F - xxx X

PART #	DEVICE FUNCTIONALITY
B	Pairs with HI-6300-xxxB – (Holt RT/MT IP Core)
C	Pairs with HI-6300-xxxC – (Holt BC/RT IP Core)
D	Pairs with HI-6300-xxxD – (Holt BC/RT/MT IP Core)
F	Pairs with HI-6300-xxxF – (Holt DO-254 DAL A Compliant RT/MT IP Core)
G	Pairs with HI-6300-xxxG – (Holt DO-254 DAL A Compliant BC/RT IP Core)
H	Pairs with HI-6300-xxxH – (Holt DO-254 DAL A Compliant BC/RT/MT IP Core)

CUSTOMER ID
Unique 3-digit customer project code, e.g. 001, 002, 003, etc.

PART #	LEAD FINISH
F	100% Matte Tin (Pb-free RoHS compliant)

PART #	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART #	PACKAGE DESCRIPTION
PQ	48 PIN PLASTIC QUAD FLAT PACK, PQFP (48PQS)

RECOMMENDED TRANSFORMERS

The HI-1587 transceiver has been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt

recommends Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO	DIMENSIONS
Premier Magnetics	PM-DB2779	Isolation	Dual 1:2.65 / 1:2.07	.675 x .400 x .185 inches
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	.625 x .625 x .250 inches

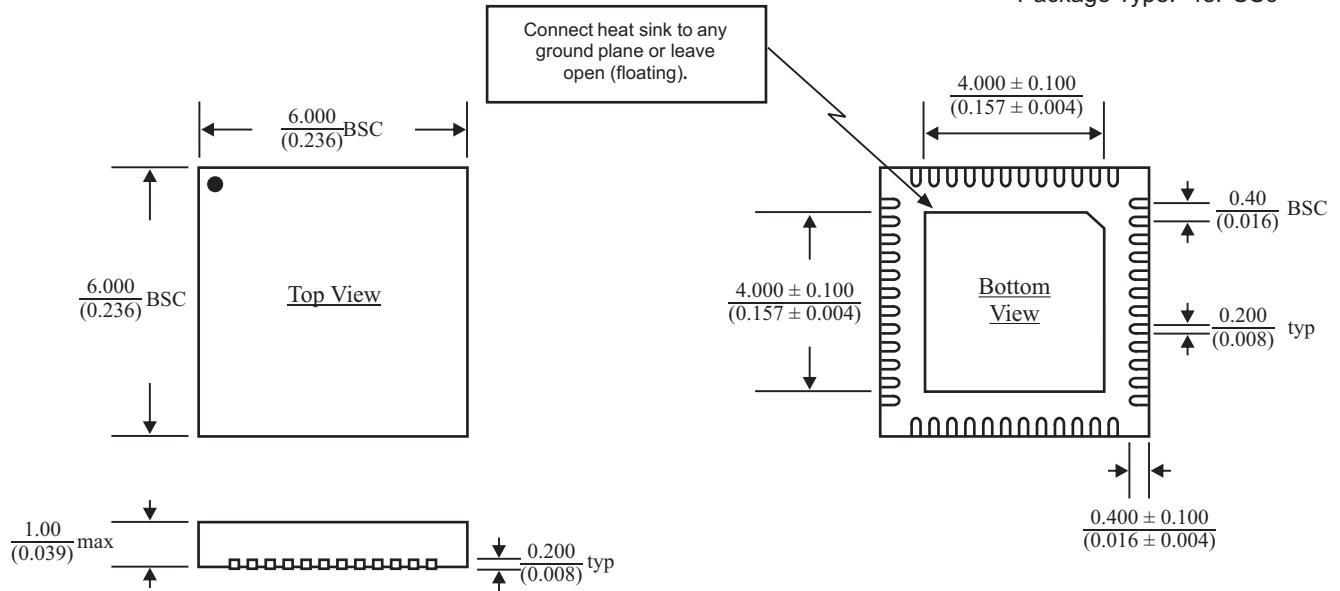
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1587	New	04/05/18	Initial Release.
	A	04/16/18	Update description of IP security module.
	B	04/23/18	Update ordering information.
	C	07/03/18	Correct typo in ordering information.
	D	02/20/19	Update note on QFN package heatsink connection.
	E	04/01/19	Add VDDIO-VLOGIC = 0.5V to Absolute Maximum Ratings. Add voltage and current parameters for all power supplies.
	F	01/10/2020	Change lead finish to NiPdAu. Change logic supply limits to 3.0V to 3.6V.
	G	05/15/2020	Remove peak output current and power dissipation from Absolute Maximum Ratings. Correct Receiver Gap Time and Receiver Enable Delay in AC Electrical Characteristics. Remove parts A and E from ordering information.
	H	09/24/2020	Remove BUSA/BIN and $\overline{\text{BUSA/BIN}}$ pins. These signals are connected to BUSA/B and $\overline{\text{BUSA/B}}$ respectively on the chip.
	J	12/04/2020	Add note on power sequencing.
	K	04/16/2021	Add 48-pin QFP package option.
	L	08/20/2021	Update Total Supply Current and Total Power Dissipation in DC Electrical Characteristics.
	M	04/14/2022	Update supply current and power dissipation numbers in DC Electrical Characteristics. Add note on Power Supply Sequencing.

48-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 48PCS6

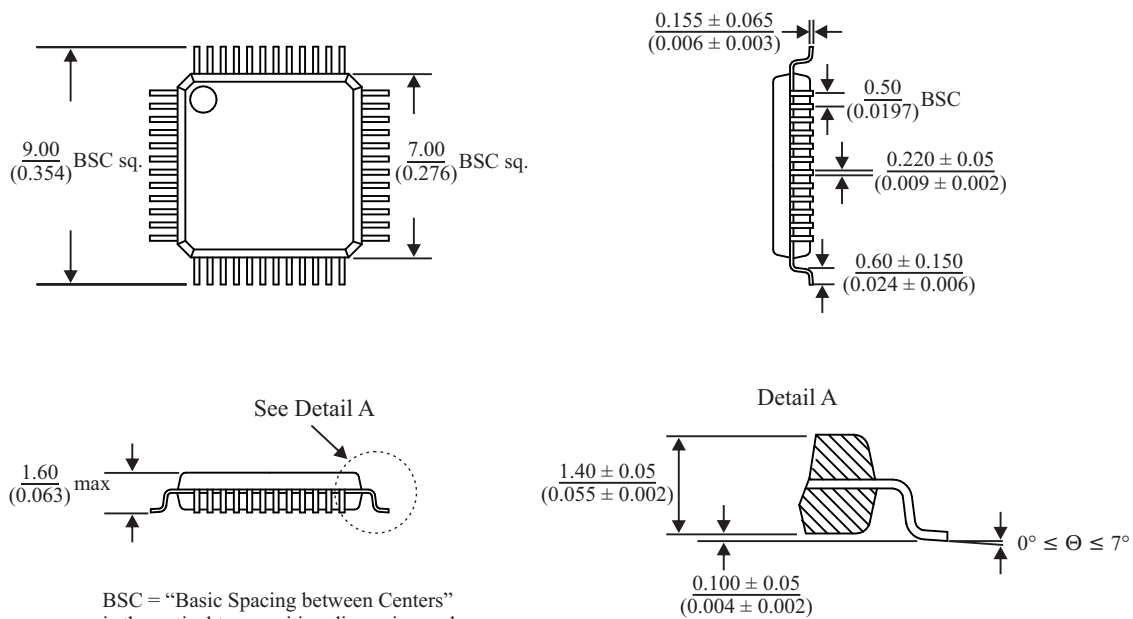


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

48 PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 48PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)